Design of 5th Order Elliptic Switched Capacitor Filter

ECE626: Analog CMOS Circuit Design

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1 Introduction

This report describes the design and simulation of a low pass switched capacitor filter for the required specifications as given in Table 1. After designing the filter with the ideal macromodels the report further discusses the effect of non idealities on the designed filter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency ((f_s))</td>
<td>15 MHz</td>
</tr>
<tr>
<td>DC gain</td>
<td>0 dB</td>
</tr>
<tr>
<td>Passband</td>
<td>0-1 MHz</td>
</tr>
<tr>
<td>Ripple in passband</td>
<td>&lt; 0.2 dB</td>
</tr>
<tr>
<td>Stopband</td>
<td>2-7.5 MHz</td>
</tr>
<tr>
<td>Gain in stopband</td>
<td>&lt;-60 dB</td>
</tr>
<tr>
<td>Minimum capacitor size</td>
<td>50 fF</td>
</tr>
</tbody>
</table>

Table 1: Design Specifications

For the given specifications required filter order was calculated using MATLAB ‘filter design toolbox’. From Table 2 we can see that since the phase information is not critical so elliptic filter will be the best choice available with minimum order.

<table>
<thead>
<tr>
<th>Filter</th>
<th>Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Butterworth</td>
<td>12</td>
</tr>
<tr>
<td>Chebyshev I</td>
<td>7</td>
</tr>
<tr>
<td>Chebyshev II</td>
<td>7</td>
</tr>
<tr>
<td>Elliptic</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 2: Requirement of filter order

2 Filter Design

For the given requirements transfer function of the elliptic filter is found to be:

\[
H(z) = \frac{0.002256z^5 - 0.002072z^4 + 0.002009z^3 + 0.002009z^2 - 0.002072z + 0.002256}{z^5 - 4.075z^4 + 6.871z^3 - 5.964z^2 + 2.657z - 0.4854}
\]  

(1)

The frequency response of the filter and the pole-zero plots are shown in Fig. 1 and Fig. 2 respectively.
Figure 1: Frequency Response of the filter with matlab and with ideal macromodels in cadence
2.1 Design of Filter Sections

Since the transfer function is of 5th order so to realize the filter we will go with the cascade design method and will break the higher order polynomials to maximum of second order system.

![Block Diagram of Cascaded Filter Sections](image)

The transfer function $H(z)$ can be expressed as cascade of one linear and two biquad sections. The individual transfer functions are given below. Gain of the overall system is divided equally between all three stages and will be taken care of in the next subsequent stages.

\[
H_1(z) = \frac{0.1312z + 0.1312}{z - 0.8054} \quad (2)
\]

\[
H_2(z) = \frac{0.1312z^2 - 0.1814z + 0.1312}{z^2 - 1.727z + 0.9082} \quad (3)
\]

\[
H_3(z) = \frac{0.1312z^2 - 0.1025z + 0.1312}{z^2 - 1.641z + 0.7359} \quad (4)
\]
The linear section, high Q biquad (HQ) and the low Q biquad (LQ) sections are shown in Fig 4, 5, and 6.

Figure 4: Schematic diagram of linear section
Figure 5: Schematic diagram of High Q Biquad section

Figure 6: Schematic diagram of Low Q biquad section
2.1.1 Dynamic Range Scaling:

After designing the filter with some initial guess of $C_1$ and $C_2$ we can see from figure 8 that all the Op-Amps have different output swings. To make the swing equal we need to go for dynamic range scaling so that all the opamps will behave similarly with uniform swing. Dynamic Range Scaling is performed in the following order:

1.) Find the peak values of one gain stage as a ratio to 0dB, call it $k$.
2.) Locate all the capacitor attached to the input and output node of that Op-Amp.
3.) Multiply the capacitors by $k$ if we want to scale the feedback capacitors else divide by $k$ for the capacitors connected to the input node of the Op-Amp.
4.) To maintain the constant current output scale the output capacitors by multiplying the capacitor values with $k$.
5.) Repeat the procedure to the rest of the gain stages, including intermittent stages.

The frequency magnitude responses after dynamic range scaling are shown in Figure 8.

![Figure 7: Op-Amp Output swing before Dynamic Range scaling](image-url)
2.1.2 Chip Area Scaling:
Since the minimum capacitance is 50 fF, all the capacitors should be scaled to that value in order to achieve the minimum die area base on capacitance alone. Because the ratios of capacitance’s stay the same, the output response should not change. The way to optimize capacitance area is:
1.) Find all the capacitors attached to the input node an Op-Amp
2.) Set the smallest capacitor to 50 fF and scale all the other capacitors to that value
3.) Repeat the process for all the other gain stages, including intermittent stages
The capacitor area optimization is easily done after the dynamic range scaling. The output response is found unchanged from what is shown in Figure 8 due to the implementation of ideal micromodels.
Then, the minimum capacitance found is scaled to 50 fF and all the other capacitors are scaled accordingly. This essentially reduces the design size.
The original values, DR scaled values and area optimized values of the capacitors are given as:
<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Initial Value</th>
<th>After DR Scaling</th>
<th>After Chip-Area Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_A$</td>
<td>1pF</td>
<td>1pF</td>
<td>0.3513pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>0.2845pF</td>
<td>0.2845pF</td>
<td>0.1000pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>0.3369pF</td>
<td>0.2845pF</td>
<td>0.1pF</td>
</tr>
<tr>
<td>$C_1$</td>
<td>0.1685pF</td>
<td>0.1423pF</td>
<td>0.05pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Initial Value</th>
<th>After DR Scaling</th>
<th>After Chip-Area Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_1$</td>
<td>0.2124</td>
<td>0.3084</td>
<td>0.3084</td>
</tr>
<tr>
<td>$k_2$</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$k_3$</td>
<td>0.1312</td>
<td>0.1884</td>
<td>0.1884</td>
</tr>
<tr>
<td>$k_4$</td>
<td>0.4366</td>
<td>0.4411</td>
<td>0.4411</td>
</tr>
<tr>
<td>$k_5$</td>
<td>0.4366</td>
<td>0.4320</td>
<td>0.4320</td>
</tr>
<tr>
<td>$k_6$</td>
<td>0.2472</td>
<td>0.2497</td>
<td>0.2497</td>
</tr>
<tr>
<td>$C_1$</td>
<td>1pF</td>
<td>1pF</td>
<td>0.2pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>1pF</td>
<td>1pF</td>
<td>0.2533pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Initial Value</th>
<th>After DR Scaling</th>
<th>After Chip-Area Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_1$</td>
<td>0.6500</td>
<td>0.3033</td>
<td>0.3033</td>
</tr>
<tr>
<td>$k_2$</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$k_3$</td>
<td>0.1876</td>
<td>0.1546</td>
<td>0.1546</td>
</tr>
<tr>
<td>$k_4$</td>
<td>0.3855</td>
<td>0.21215</td>
<td>0.21215</td>
</tr>
<tr>
<td>$k_5$</td>
<td>0.3855</td>
<td>0.7</td>
<td>0.7</td>
</tr>
<tr>
<td>$k_6$</td>
<td>0.4307</td>
<td>0.4307</td>
<td>0.4307</td>
</tr>
<tr>
<td>$C_1$</td>
<td>1pF</td>
<td>1pF</td>
<td>0.235pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>1pF</td>
<td>1pF</td>
<td>0.323pF</td>
</tr>
</tbody>
</table>

Table 3: The capacitance values and capacitance Ratio (a) linear section, (b) HQ Biquad and (c) LQ Biquad

2.2 Op-amp Macro-model

The op-amp macro-model used is shown in Fig. 9. This model can predict the effect of finite gain, bandwidth and slew rate on the operation of the circuit.

![Figure 9: Op-amp macro-model](image-url)
2.3 Estimation of Effect due to Non-idealities

2.3.1 Finite Gain of Op-amp

The finite gain of the Op-Amp introduces new terms in the transfer function and thus distorts pole locations of the filter.

Considering finite dc gain \( A \) of an op-amp, the \( Q \) of a pole pair gets altered by following formula [1,2]:

\[
\frac{1}{Q'} = \frac{1}{Q_{\text{ideal}}} + \frac{1}{\omega_o A T} \alpha
\]

\( Q' \) will shift the overall frequency response of the system. More importantly, the quality factor of each filter section also changes and the effect degrades the ripple in the pass-band.

A simple approximation for the ripple variation in the pass-band due to finite gain is:

\[
R_p = 1 + \frac{2Q}{\omega_o} \tag{6}
\]

Figure 10 shows the effect of dc gain variation on the ripple in the pass-band of the filter.

![Periodic AC Response](image)

**Figure 10:** Finite DC gain effect on passband ripple

2.3.2 Finite Bandwidth (BW) of Op-amp

The effect of finite BW manifests as modifying the transfer function in \( s \) domain by \( s(1 + \frac{s}{p}) \). Which essentially means, the straight line \( j\omega \) axis is replaced by a parabola of the form, \( \omega - \omega^2/p \). This effectively enhances \( Q \) of pole in \( s \) plane. Once we map from \( s \) to \( z \) plane, this property remains intact. This can be observed by simulation. So, typically op-amp BW should be \( > 5 \times \) sampling frequency. Very high bandwidth can cause fold-over noise. So, 5-8 seems to be an optimal choice.

Figure 11 shows the effect of bandwidth variation on the peaking in the pass-band of the filter.
2.3.3 Slew Rate (SR)

\[
SR = \omega V_{in}
\]  
(7)

If a signal is applied at band-edge with 1.5 V (p-p, differential) value, then maximum step in one time period is \([2]\),

\[
\Delta V = V_{in}\omega T \quad \Rightarrow \quad \Delta V \Delta T = 2V_{in}\omega 0.1
\]
(9)

\(\Delta T\) is the time allowed for slewing, typically it is \(< 0.1 \times \frac{T}{2}\). With given values, \(SR \approx 18\text{ V/\mu s}\).

The maximum load capacitance is \(\approx 350\text{ fF}\). So, for class A operation of op-amp, bias current should be \(> 10\mu A\).

Figure 12 shows the effect of bandwidth variation on the peaking in the passband of the filter.

Figure 11: Finite DC gain effect on passband ripple
Figure 12: Limited Slew Rate effect on transient response
2.3.4 Effect of Offset Voltage

- In the bilinear section at steady state,

\[ V_{o1,off} = (1 + \frac{C_2}{C_3})V_{off} \]  

For a 1 mV input offset, with selected component values, \( V_{o1,off} = 2 \text{ mV} \).

- For the high Q biquad, with a 1 mV input offset,

\[
\begin{align*}
V_{2m,off} &= \left(1 + \frac{k_1}{k_4}\right)V_{off} \\
V_{2,off} &= V_{off}
\end{align*}
\]

For a 1 mV input offset, with selected component values, \( V_{2m,off} = 1.699 \text{ mV} \) and \( V_{2,off} = 1 \text{ mV} \).

- For the low Q biquad, with a 1 mV input offset,

\[
\begin{align*}
V_{3m,off} &= \left(1 + \frac{k_1}{k_4}\right)V_{off} \\
V_{3,off} &= \left(\frac{k_1}{k_4} \cdot \frac{k_6}{k_5} - 1\right)V_{off}
\end{align*}
\]

For a 1 mV input offset, with selected component values, \( V_{3m,off} = 2.429 \text{ mV} \) and \( V_{3,off} = -0.120 \text{ mV} \).

The following plot (Figure 13) illustrates the outputs of each filter stage with an offset voltage of 1mV at the input of each Op-Amp. The output all settles to their respective calculated values after approximately 7 \( \mu \text{s} \).

![Figure 13: Input offset voltage effect on Op-Amp settling time](image)
2.3.5 Switch Sizing and Charge Injection

Assuming a fast clock with 50% charge distribution, then the first-order approximated charge injection from and the 3-dB bandwidth from of single switch NMOS sample-and-hold circuit can be shown to be:

The two expressions are also related to on-resistance and channel charge, and their product can be used as an approximated performance measurement:

Let the on resistance for a typical switch be $R$ and it’s charging/ discharging a capacitor of value $C$. At any phase ($\phi_1$ or, $\phi_2$), two such switches are in series with $C$.

Each phase lasts for $\approx \frac{T}{2}$. Therefore,

$$V_{final} = V_{initial} \cdot (1 - e^{-\frac{T}{RC}}) \tag{13}$$

Similarly, the feedback cap at op-amp output gets scaled by same factor.

For an error $< 0.1\%$, we need $RC < \frac{T}{15} \tag{2}$.

The largest $C \approx 0.323 \text{ pF}$. This gives,

$$R < \frac{1}{C_{max} \times 15 \times f_s} = 13.7 \text{ k}\Omega \tag{14}$$

For reduced parasitics, selecting $L = 0.25 \mu m$, $W = 0.5 \mu m$.

Using [2], the error voltage caused by charge injection is given by,

$$R_{\text{switch}} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{15}$$

$$Q_{ch} = 0.5WLC_{ox}(V_{GS} - V_{th}) \tag{16}$$

$$\Rightarrow R_{\text{switch}}Q_{ch} = \frac{0.5L^2}{\mu_n} \tag{17}$$

$$\Rightarrow Q_{ch} = \frac{7.5L^2f_sC}{\mu_n} \tag{18}$$

$$\Rightarrow V_{error} = \frac{7.5L^2f_s}{\mu_n} \approx 135 \text{ mV} \tag{19}$$

The above equation shows a clear trade-off between speed and accuracy. The overall performance is limited by on-resistance and channel charge, which is shown to be a result of electron mobility and channel length. Using minimum length maximizes both speed and accuracy, and the overall performance scales roughly with the length squared. The width and the hold capacitance, on the first-order, have no effect because doubling the width roughly doubles both the bandwidth and the charge injection error. Therefore, the width and the hold capacitance have minimum effect on the overall performance of the sampling switch.

Figure 14 shows the comparison between different switch sizes and the error in the output voltage due to their charge injection. From here it can be clearly seen that as we increase the switch size the charge injection error increases.
The op-amp used in the filter is implemented by a folded cascode structure in standard 0.25µm CMOS process. The achieved performance summary of the op amp is given below:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications</th>
<th>Typical (27°C)</th>
<th>Fast (-40°C)</th>
<th>Slow (100°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>2.5V ± 0.25V</td>
<td>2.5V</td>
<td>2.75V</td>
<td>2.25V</td>
</tr>
<tr>
<td>Load (at each output)</td>
<td>2pF ± 30%</td>
<td>2pF</td>
<td>1.4pF</td>
<td>2.6pF</td>
</tr>
<tr>
<td>Loop Gain</td>
<td>&gt;75dB</td>
<td>76.96dB</td>
<td>76.78dB</td>
<td>73.18dB</td>
</tr>
<tr>
<td>Loop UGBW</td>
<td>&gt;100MHz</td>
<td>157MHz</td>
<td>248MHz</td>
<td>88.4MHz</td>
</tr>
<tr>
<td>Loop Phase Margin</td>
<td>&gt;65°</td>
<td>70.4</td>
<td>65.3</td>
<td>76</td>
</tr>
<tr>
<td>CMFB Phase Margin</td>
<td>&gt;45°</td>
<td>94.06</td>
<td>98.78</td>
<td>103.8</td>
</tr>
<tr>
<td>Output CM Voltage</td>
<td>1.25V ± 0.1V</td>
<td>1.188V</td>
<td>1.19V</td>
<td>1.115V</td>
</tr>
<tr>
<td>Output Swing</td>
<td>&gt;1.5V&lt;sub&gt;pk&lt;pk&lt;/sub&gt;</td>
<td>1.944V</td>
<td>2.17V</td>
<td>829mV</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt;10mW</td>
<td>9.87mW</td>
<td>11mW</td>
<td>6.92mW</td>
</tr>
</tbody>
</table>

Table 4: Op-Amp Performance Summary
Figure 15: Op-Amp Schematic

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$W(\mu m)$</th>
<th>Transistor</th>
<th>$W(\mu m)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1a,b</td>
<td>170</td>
<td>M9</td>
<td>3.2</td>
</tr>
<tr>
<td>M2a,b</td>
<td>160</td>
<td>M12,M15</td>
<td>3.2</td>
</tr>
<tr>
<td>M3a,b,c,d</td>
<td>160</td>
<td>M13</td>
<td>1.06</td>
</tr>
<tr>
<td>M4a,b,c,d</td>
<td>408</td>
<td>M14</td>
<td>0.64</td>
</tr>
<tr>
<td>M5a,M5b</td>
<td>100.8</td>
<td>M16a,b</td>
<td>8</td>
</tr>
<tr>
<td>M6</td>
<td>624</td>
<td>M17a,b,c,d</td>
<td>20</td>
</tr>
<tr>
<td>M7,M10,M11</td>
<td>9.6</td>
<td>M18a,b</td>
<td>24</td>
</tr>
<tr>
<td>M8</td>
<td>1.92</td>
<td>Vdd</td>
<td>2.5V</td>
</tr>
<tr>
<td>Ibias</td>
<td>40$\mu A$</td>
<td>$C_{load}$</td>
<td>2pF</td>
</tr>
</tbody>
</table>

Table 5: Transistor Sizing
With real Op-Amp the filter is again simulated and from the figure given below we can see that the filter is meeting the required specifications with all the non-idealities of real Op-Amp.

Figure 16: Op-Amp Loop Gain response
Figure 17: Frequency Response of the filter with real and ideal op-amps

**Acknowledgment:**

To put my data in proper format I used the structure of Ankur Guha Roy’s Report.

**Appendix**

Matlab Code:

```matlab
clear all
clc

fs=15e6;
Ws=2e6/(fs/2);
Wp=Ws/2;
Rp=0.1;
```
Rs=61;

[Nbutt, Wnbutt]=buttord(Wp,Ws,Rp,Rs);
[Ncheb1, Wncheb1]=cheb1ord(Wp,Ws,Rp,Rs);
[Ncheb2, Wncheb2]=cheb2ord(Wp,Ws,Rp,Rs);
[Nellip, Wnellip]=ellipord(Wp,Ws,Rp,Rs);

[num, den]=ellip(Nellip,Rp,Rs,Wp);

H=tf(num,den,1/fs);

% Transfer function:
% 0.002256 z^5 - 0.002072 z^4 + 0.002009 z^3 + 0.002009 z^2 - 0.002072 z + 0.002256
% -----------------------------------------------
% z^5 - 4.075 z^4 + 6.871 z^3 - 5.964 z^2 + 2.657 z - 0.4854
% %
% % Sampling time: 6.6667e-08

[H, w]=freqz(num, den);
plot(w/(2*pi)*(fs), 20*log10(abs(H)));

% Pole Zero Plot
[z, p, k] = tf2zpk(num, den);

% z =
% % -1.0000
% % 0.6464 + 0.7630i
% % 0.6464 - 0.7630i
% % 0.3127 + 0.9499i
% % 0.3127 - 0.9499i
% %
% % p =
% % 0.8507 + 0.4103i
% % 0.8507 - 0.4103i
% % 0.7975 + 0.2508i
% % 0.7975 - 0.2508i
% % 0.7785
% %
% % k =
% % 0.0023

zplane(num, den);

% Factoring the transfer function
[sos, g]=tf2sos(num, den);
gg=g^(1/3);

%% sos =

zplane(num, den);
```matlab
%% Find the coefficients for the biquads (Low Q)
a0 = (gg*sos(2,3))/(sos(2,6));
a1 = (gg*(sos(2,2))/(sos(2,6)));
a2 = (gg*(sos(2,1))/(sos(2,6)));
b1 = sos(2,5)/sos(2,6);
b2 = sos(2,4)/sos(2,6);
K5LQ = (b1+b2+1)^(1/2);
K1LQ = (a0 + a1 + a2)/K5LQ;
K2LQ = a2 - a0;
K3LQ = a0;
K4LQ = K5LQ;
K6LQ = (b2 -1);

%% High Q Coefficients
a0 = gg*sos(3,3);
a1 = gg*sos(3,2);
a2 = gg*sos(3,1);
b1 = sos(3,5);
b0 = sos(3,6);
K4HQ = (((1+b0+b1)^(1/2)));
K5HQ = (((1+b0+b1)^(1/2)));
K1HQ = (a0+a1+a2)/K5HQ;
K3HQ = a2;
K6HQ = (((1-b0)/K5HQ));
K2HQ = (a2-a0)/K5HQ;

%% Linear Section
C1 = (sos(1,2)*gg)/abs(sos(1,5));
C2 = -2*C1;
C3 = (sos(1,4)/abs(sos(1,5)))-1;

[H1,w1]=freqz([gg gg],[1 -0.8054]);
[H2,w2]=freqz([gg*1.0000 gg*-1.3833 gg*1.0000],[ 1.0000 -1.7269 0.9082]);
[H3,w3]=freqz([gg*1.0000 gg*-0.7813 gg*1.0000],[ 1.0000 -1.6410 0.7359]);

H=tf(num,den,1/fs)
lin_tf=tf([gg gg],[1 -0.8054],1/fs);
HQ_tf=tf([gg*1.0000 gg*-1.3833 gg*1.0000],[ 1.0000 -1.7269 0.9082],1/fs);
LQ_tf=tf([gg*1.0000 gg*-0.7813 gg*1.0000],[ 1.0000 -1.6410 0.7359],1/fs);
```