University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

LC-3 Control Signals for Instruction Fetch and Decode

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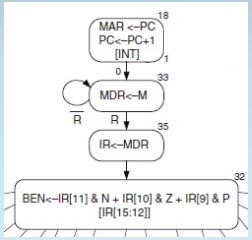
How Does the LC-3 FSM Control Fetch and Decode?

Let's work out the control signals needed for instruction fetch and decode.

The figure to the right is part of Patt and Patel Figure C.2.

The first state:



MAR ← PC, PC ← PC + 1

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What are the Load Signals?

MAR ← PC, PC ← PC + 1

Which registers change in the first state of fetch?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
fetch 1	1	0	0	0	0	0	1
fetch 2							
fetch 3							
decode							

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Look at How Bits Must Move in the Datapath

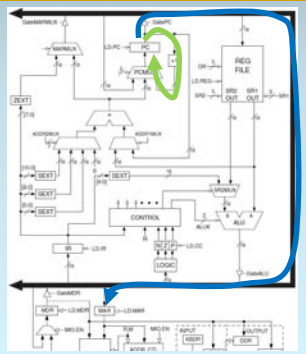
Let's look at the datapath.

We have…

MAR ← PC

and

PC ← PC + 1



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What are the Bus Gating Signals?

MAR ← PC, PC ← PC + 1

So what are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
fetch 1	1	0	0	0
fetch 2				
fetch 3				
decode				

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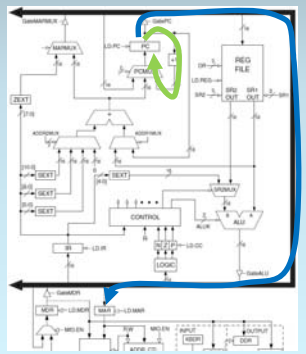
Which Muxes are Needed for the First Fetch State?

Which muxes matter?

Only PCMUX!



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What are the Mux Selection Signals?

MAR ← PC, PC ← PC + 1

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
fetch 1	00	xx	xx	x	xx	x
fetch 2						
fetch 3						
decode						

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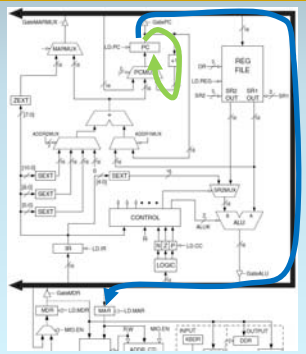
The First Fetch State Uses Neither the ALU nor Memory

Both the **ALU** and memory are unused.



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What are the ALU and Memory Signals?

MAR ← PC, PC ← PC + 1

What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
fetch 1	xx	0	x
fetch 2			
fetch 3			
decode			

Notice that MIO.EN is NOT a don't care!

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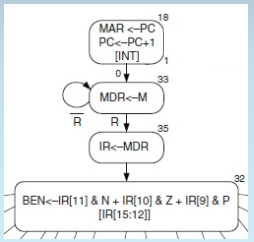
Continue with the Second Fetch State



The second fetch state:

MDR ← M[MAR]

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What are the Load Signals?

MDR ← M[MAR]

Which registers change in the second state of fetch?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
fetch 1	1	0	0	0	0	0	1
fetch 2	0	1	0	0	0	0	0
fetch 3							
decode							

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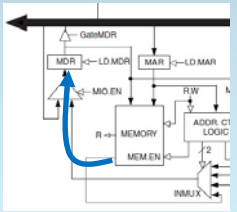
Look at How Bits Must Move in the Datapath

Let's look at the datapath.

We have…

MDR ← M[MAR]

(The mux in the datapath is used for memory-mapped I/O, which we didn't cover.)



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What are the Bus Gating Signals?

MDR ← M[MAR]

So what are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
fetch 1	1	0	0	0
fetch 2	0	0	0	0
fetch 3				
decode				

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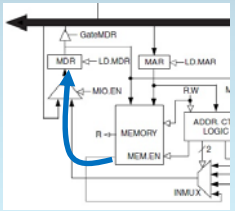
Which Muxes are Needed for the Second Fetch State?

Which muxes matter?

None of them!



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What are the Mux Selection Signals?

MDR ← M[MAR]

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
fetch 1	00	xx	xx	x	xx	x
fetch 2	xx	xx	xx	x	xx	x
fetch 3						
decode						

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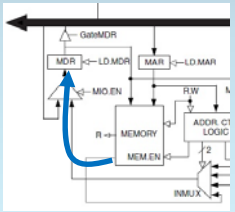
The Second Fetch State Performs a Read

Memory must perform a **read** operation.

The **ALU** is unused.



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What are the ALU and Memory Signals?

MDR ← M[MAR]

What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
fetch 1	xx	0	x
fetch 2	xx	1	0
fetch 3			
decode			

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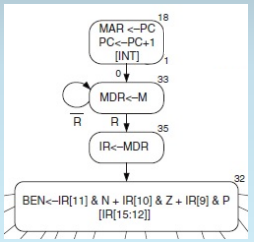
Continue with the Third Fetch State



The third fetch state:

IR ← MDR

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What are the Load Signals?

IR ← MDR

Which registers change in the third state of fetch?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
fetch 1	1	0	0	0	0	0	1
fetch 2	0	1	0	0	0	0	0
fetch 3	0	0	1	0	0	0	0
decode							

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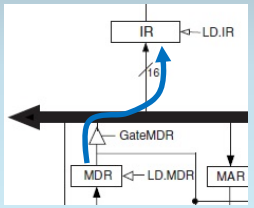
Look at How Bits Must Move in the Datapath

Let's look at the datapath.

We have…

IR ← MDR



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What are the Bus Gating Signals?

IR ← MDR

So what are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
fetch 1	1	0	0	0
fetch 2	0	0	0	0
fetch 3	0	1	0	0
decode				

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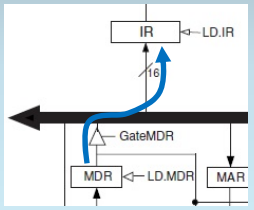
Which Muxes are Needed for the Third Fetch State?

Which muxes matter?

None of them!



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What are the Mux Selection Signals?

IR ← MDR

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
fetch 1	00	xx	xx	x	xx	x
fetch 2	xx	xx	xx	x	xx	x
fetch 3	xx	xx	xx	x	xx	x
decode						

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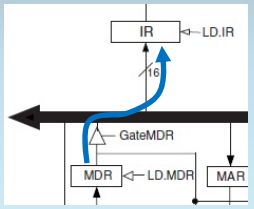
The Third Fetch State Uses Neither the ALU nor Memory

Both the **ALU** and memory are unused.



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What are the ALU and Memory Signals?

IR ← MDR

What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
fetch 1	xx	0	x
fetch 2	xx	1	0
fetch 3	xx	0	x
decode			

Notice that MIO.EN is NOT a don't care!

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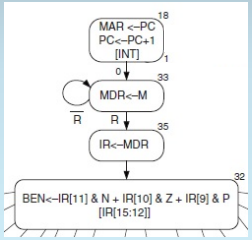
Continue with the Decode State



The decode state:

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

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What are the Load Signals?

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

Which registers change in the decode state?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
fetch 1	1	0	0	0	0	0	1
fetch 2	0	1	0	0	0	0	0
fetch 3	0	0	1	0	0	0	0
decode	0	0	0	1	0	0	0

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Look at How Bits Must Move in the Datapath

We have…

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

But the implementation
- is just some logic
- based on the condition codes (**N**, **Z**, and **P**) and the **IR**.

There's nothing to see in the datapath.

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What are the Bus Gating Signals?

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

So what are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
fetch 1	1	0	0	0
fetch 2	0	0	0	0
fetch 3	0	1	0	0
decode	0	0	0	0

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What are the Mux Selection Signals?

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
fetch 1	00	xx	xx	x	xx	x
fetch 2	xx	xx	xx	x	xx	x
fetch 3	xx	xx	xx	x	xx	x
decode	xx	xx	xx	x	xx	x

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What are the ALU and Memory Signals?

BEN ← IR[11] & N + IR[10] & Z + IR[9] & P

What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
fetch 1	xx	0	x
fetch 2	xx	1	0
fetch 3	xx	0	x
decode	xx	0	x

Notice that MIO.EN is NOT a don't care!

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Summary of Control Signals for Fetch and Decode

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
fetch 1	1	0	0	0	0	0	1
fetch 2	0	1	0	0	0	0	0
fetch 3	0	0	1	0	0	0	0
decode	0	0	0	1	0	0	0

	GatePC	GateMDR	GateALU	Gate MARMUX
fetch 1	1	0	0	0
fetch 2	0	0	0	0
fetch 3	0	1	0	0
decode	0	0	0	0

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
fetch 1	00	xx	xx	x	xx	x
fetch 2	xx	xx	xx	x	xx	x
fetch 3	xx	xx	xx	x	xx	x
decode	xx	xx	xx	x	xx	x

	ALUK	MIO.EN	R.W
fetch 1	xx	0	x
fetch 2	xx	1	0
fetch 3	xx	0	x
decode	xx	0	x

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